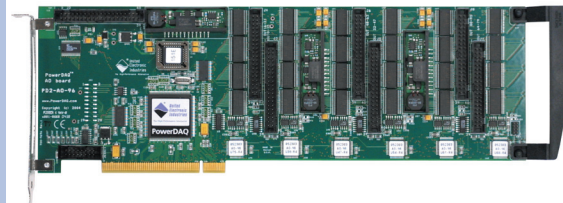


PD2-AO-96/16HS

96-Channel PCI Card for High-Speed Analog Output

- 96 analog outputs (16-bit resolution)
- 8 digital inputs; 8 digital outputs
- 100 kS/s per channel max sampling rate; high-speed waveform generation
- Three 24-bit counters/timers; three clock/interrupt lines
- User-defined power-on state
- Simultaneous channel update; update on external event
- 64k samples onboard buffer size



Supports **UEIDAQ Framework** Data Acquisition Software Library for Windows, Linux and QNX drivers available. Visit our website for more details.

General Description:

The PD2-AO-96/16HS is designed as a high-speed waveform generator. This board has the ability to output 100 kS/s per channel on all channels simultaneously using the onboard DSP memory in recycle or one-shot mode. Synchronization of the board can be performed externally or internally. All channels can be updated simultaneously. PD2-AO-96/16HS includes the DSP memory upgrade to 64K samples.

Technical Specifications:

Analog Outputs	
Number of channels	96
Resolution	16 bits
Update rate	100 kS/s per channel @ 16-bit; 200 kS/s per channel @ 12-bit; 600 kS/s aggregate in non-DMA mode; 1600 kS/s aggregate in DMA mode; 9.6 MS/s aggregate from DSP memory, regenerate waveform mode
DSP buffer size	2/64k samples (software selectable)
Type of D/A	double-buffered
Data transfer modes	DMA, interrupt, software
Accuracy	±3 LSB max
DNL	±3 LSB max
Monotonicity over temp.	15 bits, -40 to 85°C
Calibrated gain error	3mV typ, 6mV max @ ±9.8V
Calibrated offset error	1mV typ, 2mV max @ 0.0V
Output range	±10V
Output coupling	DC
Output impedance	0.15Ω max
Current drive	±5 mA min
Capacitive loads	180 pF min
Settling time	10μs to 0.003%
Slew rate	10V/μs
Gain bandwidth	1 MHz
Noise	less than 2 LSB RMS, 0-10000 Hz
Output protection	short to ground, ±15V
Power-on state	0.0000V ±5mV (default), user programmable
Gain drift	25 ppm/°C

To amplify analog outputs from ±10V to ±100V or ±115V you can use 16-channel voltage amplifiers - PD-AO-AMP-100 or PD-AO-AMP-115. The settling time for the 200V full scale is 140 μs.

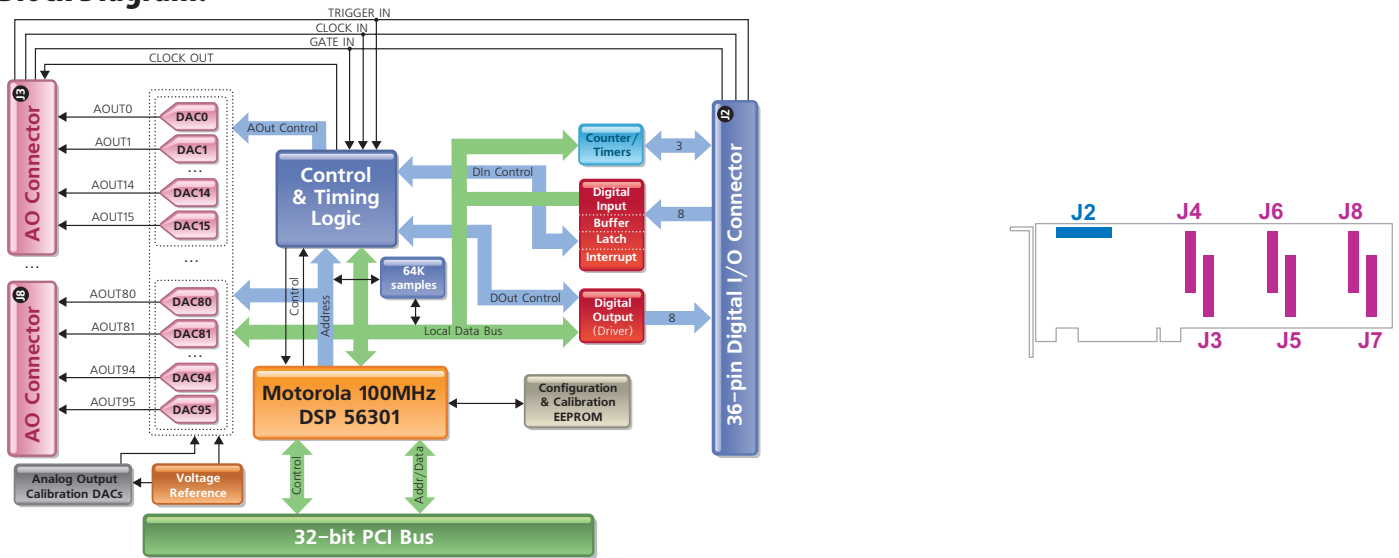
Digital I/O	
Number of channels	8 inputs, 8 outputs
Compatibility	CMOS/TTL, 2kV ESD protected
Power-on state	logic zero (default), user programmable
Data transfer modes	DMA, interrupt, software
Input termination	4.7kΩ pull-up to 5V
Output high level	3.0V typ @ -32mA, 3.4V typ @ -16mA, 4.2V @ -2mA
Output low level	0.55V max @ 64mA
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V
Counter/Timer	
Number of channels	3
Resolution	24 bits
Max frequency	16.5 MS/s for external clock, 33 MS/s for internal DSP clock
Min frequency	0.00002 Hz for internal clock, no low limit for external clock
Min pulse width	20 ns
Output high level	2.9V typ @ -4 mA
Output low level	0.5V min @ 4 mA
Protection	7 kV ESD, ±30V over/undershoot
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V

Connection Schemes:

Connector On The Board	Cable Required	Target Panel	Description
J3 - J8	PD-CBL-40	PD-STP-40	Carries 16 analog output lines to 16-channel terminal panel
J3 - J8	PD-CBL-4037	PD-STP-3716	Carries 16 analog output lines to 16-channel terminal panel*
J2	PD-CBL-37	PD-STP-3716	Carries 8 digital input and 8 output lines to 16-channel terminal panel
J3 - J8	PD-CBL-4037-INV	PD-AO-AMP-100	Carries 16 analog output lines to ±100V amplifier
J3 - J8	PD-CBL-4037-INV	PD-AO-AMP-115	Carries 16 analog output lines to ±115V amplifier
J2	PD-CBL-3650-8/8	PD2-DIO-BPLANE16	Carries digital lines to digital isolation panel for adding relays to the DIO lines

* Legacy connection scheme. Use PD-CBL-40 / PD-STP-40 combination instead.

Block Diagram:



Pinout Diagrams:

J2 — IDC-36 (male) 36-pin header:

DGND	1	2	DGND
TRMR0	3	4	TRMR2
DGND	5	6	DGND
DGND	7	8	DGND
TRMR1	9	10	+5V 200mA max
DIN0	11	12	DGND
DIN1	13	14	DOOUT0
DIN2	15	16	DOOUT1
DIN3	17	18	DOOUT2
DIN4	19	20	DOOUT3
DIN5	21	22	DOOUT4
DIN6	23	24	DOOUT5
DIN7	25	26	DOOUT6
DIN8	27	28	DOOUT7
CLOCK IN	29	30	DGND
TRIGGER IN	31	32	DGND
DGND	33	34	DGND
DGND	35	36	DGND

J3 — IDC-40 (male) 40-pin connector:

CLOCK IN	1	2	CLOCK OUT
TRIGGER IN	3	4	GATE IN
DGND	5	6	AGND
AOUT0	7	8	AGND
AOUT1	9	10	AGND
AOUT2	11	12	AGND
AOUT3	13	14	AGND
AOUT4	15	16	AGND
AOUT5	17	18	AGND
AOUT6	19	20	AGND
AOUT7	21	22	AGND
AOUT8	23	24	AGND
AOUT9	25	26	AGND
AOUT10	27	28	AGND
AOUT11	29	30	AGND
AOUT12	31	32	AGND
AOUT13	33	34	AGND
AOUT14	35	36	AGND
AOUT15	37	38	AGND
AGND	39	40	AGND

J4 — IDC-40 (male) 40-pin connector:

NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT16	7	8	AGND
AOUT17	9	10	AGND
AOUT18	11	12	AGND
AOUT19	13	14	AGND
AOUT20	15	16	AGND
AOUT21	17	18	AGND
AOUT22	19	20	AGND
AOUT23	21	22	AGND
AOUT24	23	24	AGND
AOUT25	25	26	AGND
AOUT26	27	28	AGND
AOUT27	29	30	AGND
AOUT28	31	32	AGND
AOUT29	33	34	AGND
AOUT30	35	36	AGND
AOUT31	37	38	AGND
AGND	39	40	AGND

J5 — IDC-40 (male) 40-pin connector:

NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT32	7	8	AGND
AOUT33	9	10	AGND
AOUT34	11	12	AGND
AOUT35	13	14	AGND
AOUT36	15	16	AGND
AOUT37	17	18	AGND
AOUT38	19	20	AGND
AOUT39	21	22	AGND
AOUT40	23	24	AGND
AOUT41	25	26	AGND
AOUT42	27	28	AGND
AOUT43	29	30	AGND
AOUT44	31	32	AGND
AOUT45	33	34	AGND
AOUT46	35	36	AGND
AOUT47	37	38	AGND
AGND	39	40	AGND

J6 — IDC-40 (male) 40-pin connector:

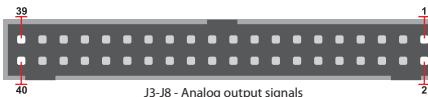
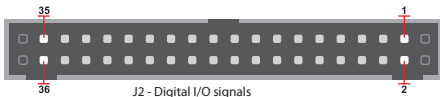
NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT48	7	8	AGND
AOUT49	9	10	AGND
AOUT50	11	12	AGND
AOUT51	13	14	AGND
AOUT52	15	16	AGND
AOUT53	17	18	AGND
AOUT54	19	20	AGND
AOUT55	21	22	AGND
AOUT56	23	24	AGND
AOUT57	25	26	AGND
AOUT58	27	28	AGND
AOUT59	29	30	AGND
AOUT60	31	32	AGND
AOUT61	33	34	AGND
AOUT62	35	36	AGND
AOUT63	37	38	AGND
AGND	39	40	AGND

J7 — IDC-40 (male) 40-pin connector:

NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT64	7	8	AGND
AOUT65	9	10	AGND
AOUT66	11	12	AGND
AOUT67	13	14	AGND
AOUT68	15	16	AGND
AOUT69	17	18	AGND
AOUT70	19	20	AGND
AOUT71	21	22	AGND
AOUT72	23	24	AGND
AOUT73	25	26	AGND
AOUT74	27	28	AGND
AOUT75	29	30	AGND
AOUT76	31	32	AGND
AOUT77	33	34	AGND
AOUT78	35	36	AGND
AOUT79	37	38	AGND
AGND	39	40	AGND

J8 — IDC-40 (male) 40-pin connector:

NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT80	7	8	AGND
AOUT81	9	10	AGND
AOUT82	11	12	AGND
AOUT83	13	14	AGND
AOUT84	15	16	AGND
AOUT85	17	18	AGND
AOUT86	19	20	AGND
AOUT87	21	22	AGND
AOUT88	23	24	AGND
AOUT89	25	26	AGND
AOUT90	27	28	AGND
AOUT91	29	30	AGND
AOUT92	31	32	AGND
AOUT93	33	34	AGND
AOUT94	35	36	AGND
AOUT95	37	38	AGND
AGND	39	40	AGND



Pin-to-Pin Mapping Diagrams:

Depending on the cable used to connect the board to different terminal panels, pins of J2, J3-J8 connectors may be remapped. Please refer to the diagrams below for detailed information about pin-to-pin mapping for PD-CBL-4037, PD-CBL-4037-INV and PD-CBL-37 cables.

PD-CBL-4037		
Pin	>	Pin
1	>	1
2	>	20
3	>	2
4	>	21
5	>	3
6	>	22
7	>	4
8	>	23
9	>	5
10	>	24
11	>	6
12	>	25
13	>	7
14	>	26
15	>	8
16	>	27
17	>	9
18	>	28
19	>	10
20	>	29
21	>	11
22	>	30
23	>	12
24	>	31
25	>	13
26	>	32
27	>	14
28	>	33
29	>	15
30	>	34
31	>	16
32	>	35
33	>	17
34	>	36
35	>	18
36	>	37
37	>	19
38	>	
39	>	
40	>	

PD-CBL-4037-INV		
Pin	>	Pin
1	>	19
2	>	37
3	>	18
4	>	36
5	>	17
6	>	35
7	>	16
8	>	34
9	>	15
10	>	33
11	>	14
12	>	32
13	>	13
14	>	31
15	>	12
16	>	30
17	>	11
18	>	29
19	>	10
20	>	28
21	>	9
22	>	27
23	>	8
24	>	26
25	>	7
26	>	25
27	>	6
28	>	24
29	>	5
30	>	23
31	>	4
32	>	22
33	>	3
34	>	21
35	>	2
36	>	
37	>	1
38	>	
39	>	
40	>	

PD-CBL-37		
Pin	>	Pin
1	>	1
2	>	20
3	>	2
4	>	21
5	>	3
6	>	22
7	>	4
8	>	23
9	>	5
10	>	24
11	>	6
12	>	25
13	>	7
14	>	26
15	>	8
16	>	27
17	>	9
18	>	28
19	>	10
20	>	29
21	>	11
22	>	30
23	>	12
24	>	31
25	>	13
26	>	32
27	>	14
28	>	33
29	>	15
30	>	34
31	>	16
32	>	35
33	>	17
34	>	36
35	>	18
36	>	37
	>	19