# DNA/DNR-DIO-405

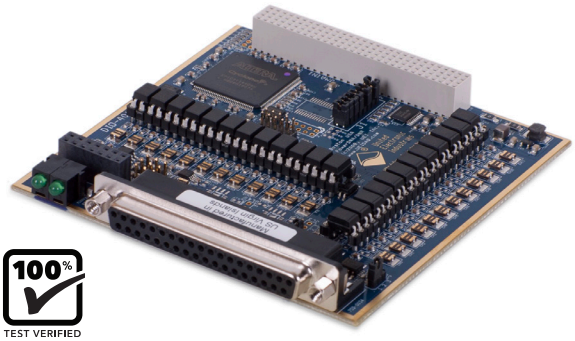
## 24-Channel Industrial Digital Input/Output Layer

- DNA-DIO-405 for use with "Cube" I/O chassis
- DNR-DIO-405 for use with RACKtangle™ I/O chassis
- 12 digital inputs, 12 digital outputs (opto-darlington output)
- Supports wide range of digital logic levels
- User-programmable hysteresis on inputs
- I/O throughput rate of 1kS/sec
- Outputs provide drive capability of 80 mA/channel
- Requires external 7-36V (24V nominal) power source

10 YEAR AVAILABILITY GUARANTEE

STANDARD WARRANTY 3 YEAR

100% TEST VERIFIED



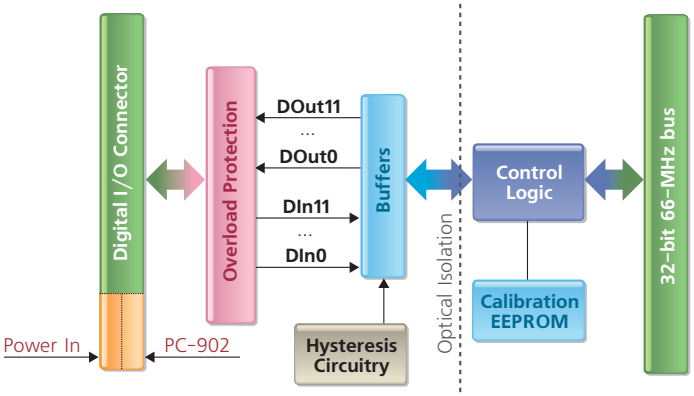
Supports **UEIDaq Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

## General Description:

The DNA/DNR-DIO-405 are digital input/output boards designed for low-speed, high-reliability isolated industrial digital I/O. The DNA-DIO-405 and DNR-DIO-405 are compatible with UEI's popular "Cube" and RACKtangle I/O chassis respectively. The boards feature 12 digital input and 12 digital output channels, I/O throughput rate of 1kHz, and 350Vrms isolation between layers. The I/O is compatible with 5-36V digital logic levels and can accept a wide range of user-supplied power (7 to 36V DC). DNA-DIO-405 (in "Cube" applications) can also be powered internally using the DNA-PC-912 power conversion layer. When a single DNA-PC-912 is used to power multiple DNA-DIO layers, total power consumption should not exceed 40W. Digital inputs on the DNA-DIO-405 use a unique programmable hysteresis feature which dramatically improves noise immunity of the input signals. Digital outputs on the DNA-DIO-405 are capable of driving up to 80mA per channel without sacrificing performance - with peak current drive capability of 200mA (2 seconds max). All digital inputs and outputs are protected with a 100mA PTC fuse and ESD/overvoltage protection device.

The DNA/DNR-DIO-405 are an ideal solution to a wide variety of data acquisition, data logging and industrial control applications that required higher than logic-level voltage ranges.

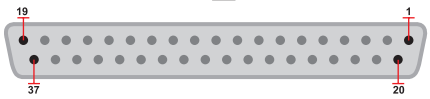
## Block Diagram:




## Pinout Diagram:

DB-37 (female)
**37-pin connector:**

| | | | |
|---|---|---|---|
| VCC | 37 | 19 | VCC |
| DGND | 36 | 18 | VCC |
| DOUT11 | 35 | 17 | DGND |
| DOUT9 | 34 | 16 | DOUT10 |
| DOUT8 | 33 | 15 | DGND |
| DOUT6 | 32 | 14 | DOUT7 |
| DOUT5 | 31 | 13 | DGND |
| DOUT3 | 30 | 12 | DOUT4 |
| DOUT2 | 29 | 11 | DGND |
| DOUT0 | 28 | 10 | DOUT1 |
| DIN11 | 27 | 9 | DGND |
| DIN9 | 26 | 8 | DIN10 |
| DIN8 | 25 | 7 | DGND |
| DIN6 | 24 | 6 | DIN7 |
| DIN5 | 23 | 5 | DGND |
| DIN3 | 22 | 4 | DIN4 |
| DIN2 | 21 | 3 | DGND |
| DIN0 | 20 | 2 | DIN1 |
| | | 1 | DGND |




**Note:** Connect external power source to **VCC** pins. All VCC and at least 3 **DGND** pins should be used to supply external power.

## Technical Specifications:

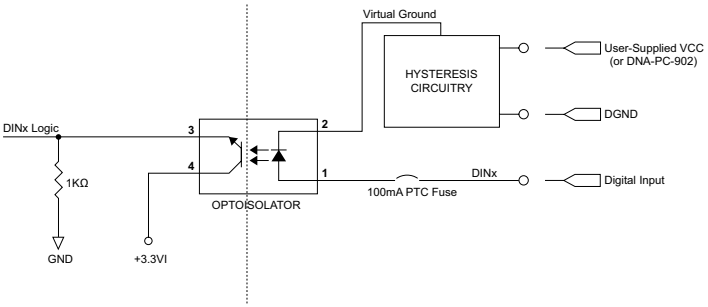
| | | | | |
|---|---|---|---|---|
| Digital Lines | 12 inputs, 12 outputs (opto-darlington) | | | |
| Logic Level | 5V - VCC | | | |
| Drive Capacity | 80 mA per channel continuous;<br>200mA per channel maximum peak | | | |
| FIFO Size | Input: 512 samples; Output: 512 samples | | | |
| Default Hysteresis Values | Lower DAC limit: 200<br>Upper DAC limit: 300 | | | |
| Input High Voltage:<br>(with default hysteresis) | @7V | @12V | @24V | @36V |
| | 4.5V | 4.75V | 10.5V | 13V |
| Input Low Voltage:<br>(with default hysteresis) | @7V | @12V | @24V | @36V |
| | 4.25V | 4V | 6.75V | 8.75V |
| Output High Voltage: | @7V | @12V | @24V | @36V |
| | 6V | 11.2V | 22.8V | 34.1V |
| Output Low Voltage: | 10kΩ pull-down resistor to ground | | | |
| Input Protection | ±40V over/under voltage, 7kV ESD | | | |
| Output Protection | 100mA resettable PTC fuse | | | |
| Internal Sampling Rate | 2 kHz | | | |
| I/O Throughput Rate | 1 kHz max | | | |
| Power Requirements (VCC) | 7-36V (24V nominal) - external source<br>or DNA-PC-912 internally | | | |
| No-load Power Consumption<br>(all outputs drving Logic 0) | @7V | @12V | @24V | @36V |
| | 0.5W | 0.6W | 0.8W | 1.6W |
| No-load Power Consumption<br>(all outputs driving Logic 1) | @7V | @12V | @24V | @36V |
| | 0.7W | 1.0W | 2.5W | 3.5W |
| Physical Dimensions | 3.875" x 3.875" (98 x 98 mm) | | | |
| Operating Temp. Range | Tested -40 to +85 °C | | | |
| Operating Humidity | 0 - 95%, non-condensing | | | |
| Isolation | 350Vrms | | | |
| Shock *IEC 60068-2-27*<br>*IEC 60068-2-64* | 100 g, 3 ms half sine, 18 shocks @ 6 orientations<br>30 g, 11 ms half sine, 18 shocks @ 6 orientations | | | |
| Altitude | 120,000 ft | | | |
| MTBF | > 600,000 hours | | | |

## Connection Options:

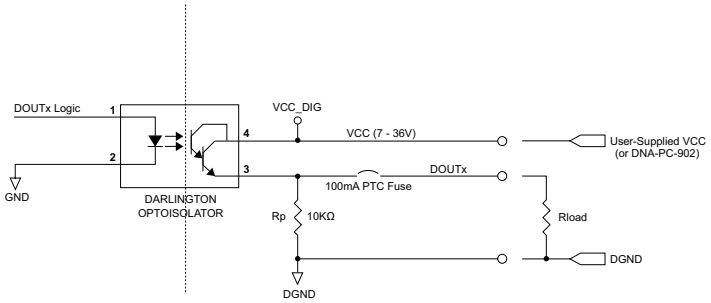
| Cable | Screw Terminal Panel | Description |
|---|---|---|
| DNA-CBL-37S | DNA-STP-37 | Shielded cable connection to 37-way terminal panel. |
| DNA-CBL-37 | DNA-STP-37 | Ribbon cable connection to 37-way terminal panel. |

# Channel Diagrams:

**Simplified Input Channel Diagram**

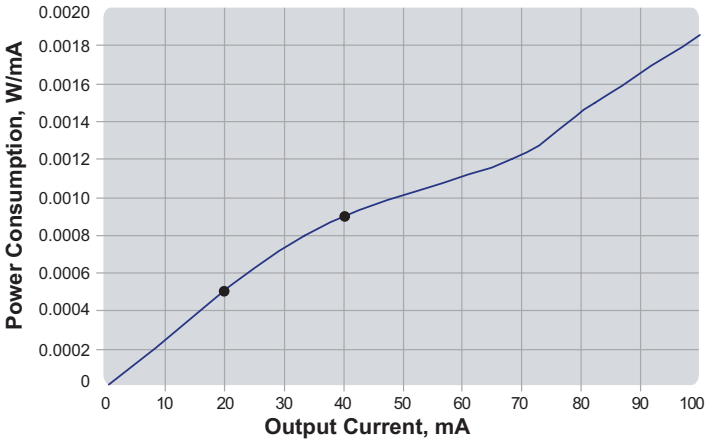



**Simplified Output Channel Diagram**




# Power Consumption:

**Power Consumption vs. Output Current**



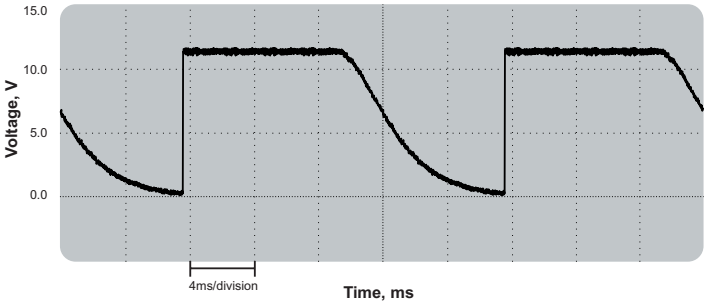

**Total Layer Power Consumption Example:**
(All outputs driving Logic High)

- VCC = 24V
- 2 outputs @ 40mA (0.009 W/mA)
- 10 outputs @ 20mA (0.005 W/mA)

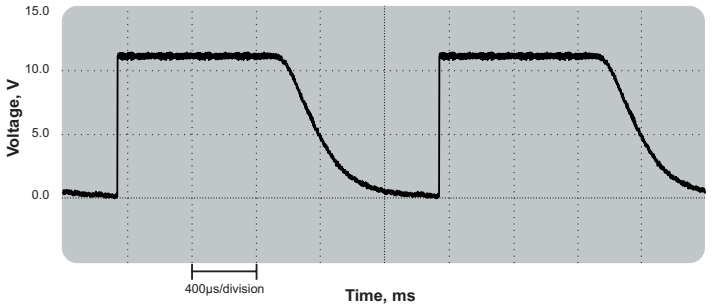
P = 2.5W + ((2 x 40) x 0.009) + ((10 x 20) x 0.005) = **4.22W**

# Falling Edge:

**5.1ms - Falling Edge of a Single Output Channel at 50Hz (No-Load Output[4])**




**406µs - Falling Edge of a Single Output Channel at 500Hz (200Ohms-Load Output)**




[4] A pull-down resistor (Rp 10KΩ) on the output is added to provide stable signal level when driven with Logic "0", but it can't guarantee that output voltage will drop to 0V. That - will be achieved with user load.

# Hysteresis Setup:

Hysteresis is a very powerful feature that improves noise immunity on the digital inputs in industrial environments. Hysteresis on the DNA-DIO-405 is implemented as follows:

Two user programmable digital-to-analog converters are used to set upper and lower limits for the hysteresis function. These D/A converters are referred to as Lower limit DAC and Upper limit DAC. DAC outputs are connected to the multiplexer and then amplified using the high-speed amplifier. The amplifier drives the 'virtual' ground of the optical isolator.

- All inputs initially read while optical isolators are driven with virtual ground level that corresponds to the value of Lower DAC
- Another read is performed while the optical isolators are driven with a virtual ground level that corresponds to the value of Upper limit DAC
- If digital input values from both reads are the same – the input signal state is assigned to the last read value, otherwise input signal state is unchanged
- This process repeats itself 1000 times a second

To set the hysteresis values, programm the Lower and Upper DACs with an arbitrary integer number from 0 to 1023. The value of the Upper DAC should always be greater than LowerDAC by at least 50. Actual DAC values should be selected based on user requirements using the formula below:

$$\text{DAC Value}^{5} = \frac{\text{Desired Hysteresis Voltage}}{\text{VCC} \times 800}$$

[5] Since different optocouplers have different characteristics, this formula gives you approx ±10% accuracy.